

<b>INFORMATION DISCLOSURE CITATION</b> PTO-1449	Customer Number: <b>26615</b>	<b>ATTORNEY'S DKT No.</b> <b>H1164</b>	<b>APPLICATION NO.</b> <b>Unassigned 10/633,503</b>
		<b>APPLICANT(S)</b> <b>Zoran Krivokapic et al.</b>	
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## **U.S. PATENT DOCUMENTS**

## **FOREIGN PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

<i>BK</i>	Digh Hisamoto et al., "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.
<i>BK</i>	Yang-Kyu Choi et al., "Sub-20nm CMOS FinFET Technologies," 2001 IEEE, IEDM, pages 421-424.
<i>BK</i>	Xuejue Huang et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886.
<i>BK</i>	Xuejue Huang et al., "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70.
<i>BK</i>	Yang-Kyu Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.

EXAMINER	DATE CONSIDERED
Bonnie Keboda	10/27/2007

**EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).